15.57/6348

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#7 Election + Amdt a FJONES 1-22-03

In re the Application of Tomoyuki Furuhata
Serial No.: 10/014,584
Filing Date: December 14, 2001
For: SEMICONDUCTOR DEVICES HAVING A NON-VOLATILE MEMORY TRANSISTOR AND METHODS FOR MANUFACTURING THE SAME

Group Art Unit: 2826

Examiner: Mandala, Victor A.

FAX RECEIVED
JAN 16 2003
TECHNOLOGY CENTER 2800

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

In response to the Election/Restriction Requirement dated December 16, 2002, the response being due by January 16, 2003, Applicant has enclosed herewith a Response to Election/Restriction Requirement and Amendment. It is believed that no fees are due in connection with this paper. If, for any reason, additional fees are required, please charge them to deposit account 50-0585. A duplicate copy of this transmittal is enclosed.

Respectfully submitted,

Alan S. Raynes

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent & Trademark Office at facsimile number (703) 872-9318 on January 16, 2003.

Alan S. Raynes

Alan S. Raynes

January 16, 2003
Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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RESPONSE TO ELECTION/RESTRICTION REQUIREMENT AND AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sirs:

In response to the Election/Restriction Requirement dated December 16, 2002, the response being due by January 16, 2002, please enter and consider the following.

IN THE CLAIMS:

Please amend claims 10 and 25 as follows:

a1

10. (amended) A semiconductor device having a non-volatile memory transistor, comprising a non-volatile memory transistor including a semiconductor layer, a floating gate disposed above the semiconductor layer, and a control gate formed to extend above a portion of the floating gate, wherein a conduction layer is provided vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.

a2

25. (amended) A method for manufacturing a semiconductor device having a non-volatile memory transistor, comprising:

forming a floating gate above a semiconductor layer;

forming a control gate that extends above a portion of the floating gate; and

forming a conduction layer vertically above the floating gate at least in a region where the control gate is not disposed vertically above the floating gate.